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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/724,865	11/28/2000	Stephen M. Trimberger	X-805-2 US	8383

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EXAMINER	
TRIEU, LAURENT L	

ART UNIT	PAPER NUMBER
2137	2

DATE MAILED: 04/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/724,865	TRIMBERGER ET AL.	
	Examiner	Art Unit	
	Laurent L Trieu	2137	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 November 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☒ Claim(s) *1* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 1 is objected to because of the following informalities: The acronym "PLD" is not defined in the claim statement. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1-5 are rejected under 35 U.S.C. 102(b) as being anticipated by Curd et al., US Patent 5,838,901, hereafter referred to as Curd.

Regarding claim 1 –

- Placing the PLD into a printed circuit board - Curd discloses, "PLDs that can be programmed, erased, and verified in-system, that is, while these devices are soldered into place on the circuit board..." (Column 1, lines 20-22)
- Testing the printed circuit board using the JTAG port of the PLD – Curd discloses, "the ability to access all the above functions and features via a standard interface, such as the IEEE Standard 1149.1 Standard Test

Access Port and Boundary-Scan Architecture" (Column 4, lines 48-51) where IEEE 1149.1 is the JTAG port.

- Loading the decryption keys into the memory using the JTAG port – Curd discloses, "the input key is stored to input key register" (Column 3, lines 54-55) and "the data protect override key register is programmable, thereby allowing the stored value in that register to change from device to device and from program to program" (Column 4, lines 1-4)

Regarding claim 3 – Curd discloses, "This operation may be accomplished via an external software-driven read operation or an internal hardware-driven test circuit..." (Column 3, lines 40-42).

Regarding claims 4 and 5 – Curd discloses, "the IEEE Standard 1149.1 Standard Test Access Port and Boundary-Scan Architecture" (Column 4, lines 48-51) where IEEE 1149.1 is the JTAG port and "PLDs that can be programmed, erased, and verified in-system, that is, while these devices are soldered into place on the circuit board..." (Column 1, lines 20-22).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Patent No. US 6,366,117 B1 to Pang et al. teaches about loading a decryption key into the PLD. Patent No. US 6,704,889 B2 to Veenstra et al. teaches

using JTAG port for debugging programmable logic devices. Patent No. US 6,369,855 B1 discusses loading a key for decryption.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Laurent L Trieu whose telephone number is 703-305-0712. The examiner can normally be reached on M-F 7AM-4PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Greg Morses can be reached on 703-308-4789. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LLT
Art Unit 2137
01 April 2004

GREGORY MORSE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100